REMARKS

Claims 1-12/14 are pending of which claims 1 and 7 are independent. For the following reasons, this application should be considered in condition for allowance and passed to issue.

The Examiner acknowledges the election of species I (Claims 1-11 and 13-14). The Examiner, however, withdraws claim 6 from consideration, since claim 6 recites the limitation of the non-elected species II.

The Office Action rejects claim 7 under 35 U.S.C. §102(e) as being anticipated by Tamaki (U.S. Patent No. 6,061,282); and rejects claims 1-3, 5, 8, 9, 11, 13 and 14 under 35 U.S.C. §103(a) as being unpatentable over Tamaki ("as applied to claim 7"); and further in view of Ungar (U.S. Patent No. 5,563,524). The rejections are respectfully traversed.

Tamaki and Ungar fails to disclose or suggest a semiconductor integrated circuit testing method and apparatus configured to generate and apply a measuring signal to all pins of a semiconductor integrated circuit and correct timing thereof, as claims 1 and 7 recite. A more in depth analysis of the claims is provided below.

Claim 7 has been amended for clarification purposes only, as it recites a "single means." Claim 7 incorporates a signal generator element to make explicit unique and novel features of the invention. No new matter has been entered.

Rejection of Claim 7 Under §102(e) as being anticipated by Tamaki

Amended claim 7 is reproduced below for convenient reference.

7. A semiconductor integrated circuit testing apparatus for testing signal wiring lengths connecting to all pins of a semiconductor integrated circuit, comprising:

a signal generator configured to generate a measuring signal and to transmit the measuring signal to all pins of the semiconductor integrated circuit; and

correcting means for correcting input waveform timing based on measurements of the measuring signal.

In rejecting claim 7, the Examiner correlates the claimed correcting means with the memory core 2, logic circuit 3, and clock buffer 5 of Fig. 1 of Tamaki. The Examiner relies on the text at cols. 4-5, line 65-3, as allegedly disclosing the means for correcting input waveform timing of a measure signal. The Examiner further references col. 4, lines 23-26, and alleges the cited text discloses that the measuring signal is "applied to all pins of the semiconductor integrated circuit", as claim 1 recites. The Examiner correlates logic circuit 3 with the claimed semiconductor and integrated circuit of claim 1. We respectfully disagree with this interpretation.

Tamaki discloses a circuit to test delay time on read data signal line 302 connected between memory core 2 and logic circuit 3 without elevating the frequency of the clock signal. To accomplish this, logic circuit 3 generates a logic circuit clock signal, which is in phase with the internal clock signal 501 of the semiconductor device, in a normal mode. In a test mode, the logic circuit 3 generates a clock signal phase opposite to the internal clock signal 501. With a change in the period of the clock signal, it is possible to measure the delay time on the signal line 302 between the memory core 2 and the logic circuit 3.

In particular, when in a normal mode, memory core 2 and logic circuit 3 operate in synchronism with the rising edge of the internal clock signal 501. On the other hand, when

in a test mode, the clock control circuit 40 (which is part of the logic circuit 3) outputs a clock signal 322 which is phase opposite to that of the internal clock 501. The oppositely phased clock signal 322 is applied to the latch group 32. As a result, data read from the memory core 2 is latched in synchronism with the falling edge of the internal clock 501 instead of the rising edge. Thus, it is possible to measure delay time by changing the high level width and low level width of the clock signal without changing the frequency of the clock signal.

Tamaki discloses a method and apparatus for measuring only the delay time on the memory data signal line 302. Tamaki fails to address how one would adjust characteristics of the semiconductor memory 1 to compensate for delay time between memory core 2 and the logic circuit 3.

By contrast, claim 7 and dependent claims therefrom are distinguishable for the following reasons:

First, claim 7 recites "correcting means". Tamaki fails to address how the delay time between the memory core 2 and logic circuit 3 would be corrected.

Claim 7 goes on to recite correcting means "for correcting input waveform timing based on measurements of measuring signal..." The Examiner correlates the claimed measuring signal with the signal transmitted between the memory core 2 and the logic circuit 3 along data line 302. As mentioned, Tamaki fails to disclose or suggest a method or apparatus for correcting input waveform timing based on delay along data line 302.

Finally, claim 7 also recites "a signal generator configured ... to transmit the measuring signal to all pins of the semiconductor integrated circuit." The Examiner correlates the claim semiconductor integrated circuit with the logic circuit 3 of Tamaki.

While one could construe a logic circuit as a semiconductor integrated circuit, the logic circuit 3 of Tamaki is without pins. Further, Tamaki merely addresses the delay time only between memory core 2 and logic circuit 3 along delay line 302. Under the Examiner's interpretation, the logic circuit 3 would also include a "pin" receiving a signal from test mode discriminator bus line 401, a "pin" transmitting a signal along write-data/control signal 301 to memory core 2, a "pin" receiving an internal clock signal from the bus 501, a "pin" transmitting output data to external port 12, and a "pin" receiving control signal/input data from port 11. Tamaki, however, only detects (not corrects) delay along data line 302, but does not address delay times connecting to any of the other "pins" or correction thereof, as just explained. Hence, Tamaki fails to disclose or suggest "correcting means" limitations, as claim 7 recites.

Claim 7 is patentable over Tamaki. Claims dependent therefrom are patentable at least based on their dependency to allowable claims 7 and for the reasons discussed above. Withdrawal of the anticipation rejection is respectfully solicited.

Rejections of claims 1-3, 5, 8, 9, 11, 13 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Tamaki in view of Ungar

The Examiner's does not explicitly address claim 1, but states that the testing apparatus of Tamaki and Ungar in combination will provide recited method steps. We respectfully disagree.

Tamaki and Ungar fail to disclose applying "a measuring signal to all pins of a semiconductor integrated circuit," as claimed 1 recites. Tamaki merely tests the read data

applied via bus 302 to the logic circuit 3. There is no disclosure or suggestion of applying a measuring signal to all pins of the logic circuit 3, as the Examiner seems to suggest.

Ungar illustrates an apparatus for testing units, which are illustrated by the Unit Under Test (UUT) 14 component. The testing apparatus connects to UUT 14 via interface 22. Ungar illustrates a high level block diagrams of the UUT, but does not disclose or suggest the step of "causing a tester to generate or measuring signal to all pins of the integrated circuit", as claim 1 recites. Figure 2 illustrates the UUT 14, which is designated by IC. Referring back to Fig. 1, the host computer 12 and circuitry connected therebetween test the UUT 14. Computer 12 forms the analysis for the appropriate test and performs the test on the UUT 14. The IC corresponds to the actual semiconductor integrated circuit under test. As illustrated, the tester only connects to certain pins of all the pins of the IC. That is, the host computer 12 and intervening circuitry transmit signals to a limited number pins of the IC.

By contrast, claim 1 recites a step of "causing a tester to generate a measuring signal to all pins of a semiconductor integrated circuit." Neither Tamaki nor Ungar discloses such a configuration whereby measuring signals are generated to all pins of a semiconductor integrated circuit, as claimed.

The Examiner states that it would have been obvious "to modify the testing apparatus of Tamaki with clock generating means of Ungar in order to make universal test apparatus [lines 61-67 of column 1] for testing electrical circuits [lines 32-37 of column 1 and Fig. 1]."

It is unclear how Tamaki could be modified with "the clock generating means of Ungar in order to make universal test apparatus." The text cited by the Examiner does not address a clock generating means.

It is well settled case law precedent that there must be some motivation to combine on the objective evidence of record. The Examiner has made a conclusionary statement not supported by any evidence.

Further, it is well settled case law and precedent that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. Tamaki is configured to measure delay time without elevating the frequency of the clock signal. The clocks of Ungar are provided to synchronize the host computer 12 with the UUT 14. If the clock generating means were incorporated into the device of Tamaki, Tamaki would become inoperable for its intended purpose. The device of Tamaki is configured to produce a phase opposite clock signal. The clock generating means of Ungar is not configured in this manner. It is unclear how a clock signal of Ungar synchronized with the internal clock signal of Tamaki could be used to detect delay times and generate a phase opposite clock signal. For the above reasons, the obviousness rejection is inappropriate.

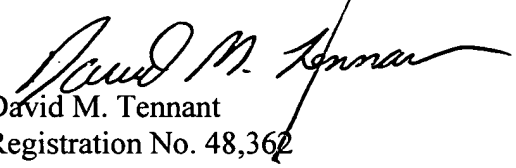
Claim 1 is patentable over Tamaki in view of Ungar as neither reference discloses or suggests the features of claim 1. Claim 7 not specifically rejected under the obviousness rejection is also patentable for the same reasons. Dependent claims cited under the obviousness rejection are patentable at least based on their dependency to either of claims 1 or 7. Withdrawal of the obviousness rejection is respectfully solicited.

In light of the remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this response or the application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX SHOWING CHANGES MADE

IN THE CLAIMS:

Claim 7 has been amended as follows:

7. (Amended) A semiconductor integrated circuit testing apparatus for testing signal wiring lengths connecting to all pins of a semiconductor integrated circuit, comprising:

a signal generator configured to generate a measuring signal and to transmit the measuring signal to all pins of the semiconductor integrated circuit; and

correcting means for correcting input waveform timing based on measurements of [a] the measuring signal.

of which

at input or output from DUT